

CLAIMS:

1. A circuit arrangement (100; 102; 104; 106) having at least one phase locked loop (40), comprising
- at least one phase detector (44) for detecting phase information of at least one analog input signal (50; 50'), in particular following the arrival of at least one rising edge and/or falling edge of at least one analog input signal (50; 50'),
 - at least one loop filter (30), to which the output signal (56) which is output by the phase detector (44) can be fed, for determining at least one increment (24), and
 - at least one ramp oscillator (46), to which the increment (24) which is output by the loop filter (30) can be fed,
- 10 characterized in that
- the phase locked loop (40) is essentially digital and for this reason may have at least one time-to-digital converter (42), to which at least one system clock (52) can be fed, for digitizing the input signal (50; 50'), in particular the phase of the input signal (50; 50'),
 - the phase detector (44) can be fed the output signal (54), in particular the
- 15 additional phase information, of the time-to-digital converter (42) and also at least a first output signal (62a), in particular at least one status signal, of the ramp oscillator (46), and
- at least one frequency detector (48) can be fed at least a second output signal (64), in particular at least one overflow pulse, of the ramp oscillator (46) and outputs frequency information (58) to the loop filter (30), which may also be assigned to, at least one
- 20 frequency locked loop (10).
2. A circuit arrangement as claimed in claim 1, characterized in that
- at least one splitter unit (70), in particular signal splitter, which can be fed
 - the increment (24) of the loop filter (30),
 - the first output signal (62b) of the ramp oscillator (46) and
 - the second output signal (64) of the ramp oscillator (46),
- 25 determines there from at least one digital output signal (80), in particular the digital phase of at least one digital output signal (80), and
- at least one digital-to-time converter (72), which can be fed the second output

signal (64) of the ramp oscillator (46), converts the digital output signal (80) into at least one analog, in particular time-dependent, output signal (82; 82').

3. A circuit arrangement as claimed in claim 1 or 2, characterized in that
- 5 - at least one analog phase locked loop (74), in particular for multiplying the output frequency, is connected downstream of the digital-to-time converter (72), and
- the output signal (84) of the analog phase locked loop (74) passes to at least one frequency generator (76), in particular to at least one frequency splitter, in order to generate at least one output signal (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') of the
- 10 circuit arrangement (100; 106).
4. A circuit arrangement (102) as claimed in claim 3, characterized in that the phase locked loop (40) has
- at least a second phase detector (38) which can be fed
- 15 - the first output signal (62a) of the ramp oscillator (46) and
- at least one output signal (86d) of the output signals (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') sent out by the frequency generator (76), and
- at least a fourth adder (32), connected between the first phase detector (44) and the loop filter (30), for adding the output signal (56) of the first phase detector (44) to the in
- 20 particular negative output signal (38a) of the second phase detector (38).
5. A circuit arrangement as claimed in claim 4, characterized in that the phase locked loop (40) has at least a second time-to-digital converter (36)
- which can be fed the output signal (86d) of the frequency generator (76) and
- 25 - the output signal (34) of which can be fed to the second phase detector (38).
6. A circuit arrangement (104) as claimed in at least one of claims 3 to 5, characterized by
- at least a first switching element (92) connected upstream of the time-to-digital
- 30 converter (42) and the phase detector (44), the output signal (92a) of which first switching element can be switched as a function of at least one switching signal (90) between the input signal (50; 50') and at least one output signal (86d) of the output signals (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') sent out by the frequency generator (76),
- at least a second switching element (94) connected between the phase detector

(44) and at least a first register element (96), assigned to the input signal (50; 50'), and at least a second register element (98), assigned to the output signal (86d) of the frequency generator (76), and

- at least a fourth adder (32), connected upstream of the loop filter (30), for adding the output signal (96a) of the first register element (96) to the in particular negative output signal (98a) of the second register element (98),

wherein

- as a function of the switching signal (90), the input (96i) of the first register element (96) or the input (98i) of the second register element (98) can be fed the output signal (56) of the phase detector (44) by the second switching element (94),
- as a function of the negated switching signal (90), the first input (32i1) of the fourth adder (32) can be fed the first output signal (94a1) of the second switching element (94) by the first register element (96), and
- as a function of the switching signal (90), the second input (32i2) of the fourth adder (32) can be fed the second output signal (94a2) of the second switching element (94) by the second register element (98).

7. A circuit arrangement as claimed in at least one of claims 1 to 6, characterized in that

- the frequency locked loop (10) has at least one increment module (12), in particular at least one increment generation unit, and
- at least one adaptation unit (14) is connected between the increment module (12) and the loop filter (30), which adaptation unit can be fed the increment (24) which is output by the loop filter (30), is designed to provide at least one adaptive algorithm and outputs at least one output signal (22).

8. A circuit arrangement as claimed in at least one of claims 1 to 7, characterized in that the loop filter (30) has

- at least a first proportional element (300) for multiplying the output signal (56) of the phase detector (44) by at least one proportional coefficient or proportional factor (K_p),
- at least one proportional path (320),
- at least one integral path (322), and
- at least a first adder (314) for adding the output signal (330) of the proportional path (320) to the output signal (350) of the integral path (322),

wherein the integral path (322) has

- at least a second proportional element (304) for multiplying the output signal (330) of the first proportional element (300) by the proportional coefficient or proportional factor (K_p),

5 - at least one integral element (306) for multiplying the output signal (340) of the second proportional element (304) by an integral coefficient or integral factor (K_i) and

- at least one integrator (308, 310, 312) intended to integrate the output signal (342) of the integral element (306), said integrator

10 -- having at least a third adder (308) for adding the output signal (342) of the integral element (306) to the output signal (58) of the frequency detector (48) and to the feedback output signal (350) of the integrator (308, 310, 312),

- having at least one integral value limiter (310) for limiting the output signal (346) of the third adder (308) and

- having at least one delay element (312).

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9. A circuit arrangement as claimed in at least one of claims 1 to 8, characterized in that

- the output signal (360) of the first adder (314) is formed as a function of the respective operating mode (26) of the phase locked loop (40)

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- either as claimed in claim 8

- or by feeding to the integral path (322) the output signal (22) of the adaptation unit (14) while at the same time feeding to the proportional path (320) at least one vanishing signal (332),

25 - at least one frequency limiter (316) for limiting the frequency of the output signal (360) of the first adder (314) is connected downstream of the first adder (314), and

- at least a second adder (318) for adding the output signal (362) of the frequency limiter (316) to at least one nominal increment signal (364) is connected downstream of the frequency limiter (316).

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10. A method of locking onto and/or processing data, in particular audio, T[ele]V[ision] and/or video data, by means of at least one phase locked loop (40), wherein

- phase information is detected by means of at least one phase detector (44), in particular following the arrival of at least one rising edge and/or falling edge of at least one analog input signal (50; 50'),

- at least one increment (24) is determined by means of at least one loop filter (30), to which the output signal (56) which is output by the phase detector (44) is fed, and
 - at least one ramp oscillator (46) is fed the increment (24) which is output by the loop filter (30),
- 5 characterized in that
- the phase locked loop (40) is essentially digital, wherein the input signal (50; 50'), in particular the phase of the input signal (50; 50') can be digitized by means of at least one time-to-digital converter (42), to which at least one system clock (52) is fed,
 - the phase detector (44) is fed the output signal (54), in particular the additional
- 10 phase information, of the time-to-digital converter (42) and also at least a first output signal (62a), in particular at least one status signal, of the ramp oscillator (46), and
- at least one frequency detector (48) is fed at least a second output signal (64), in particular at least one overflow pulse, of the ramp oscillator (46) and outputs frequency information (58) to the loop filter (30), which in particular is also assigned to at least one
- 15 frequency locked loop (10).
11. A method as claimed in claim 10, characterized in that
- at least one splitter unit (70), in particular signal splitter, which is fed
 - the increment (24) of the loop filter (30),
- 20
 - the first output signal (62b) of the ramp oscillator (46) and
 - the second output signal (64) of the ramp oscillator (46),
 determines there from at least one digital output signal (80), in particular the digital phase of at least one digital output signal (80),
- at least one digital-to-time converter (72), which is fed the second output
- 25 signal (64) of the ramp oscillator (46), converts the digital output signal (80) into at least one analog, in particular time-dependent, output signal (82; 82'),
- the output frequency is multiplied by means of at least one analog phase locked loop (74) which is connected downstream of the digital-to-time converter (72), and
 - the output signal (84) of the analog phase locked loop (74) passes to at least
- 30 one frequency generator (76), in particular to at least one frequency splitter, in order to generate at least one output signal (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') of the circuit arrangement (100; 106).

12. A method as claimed in claim 11, characterized in that
- phase information of at least one output signal (86d) of the output signals (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') sent out by the frequency generator (76) is determined and output by at least a second phase detector (38) as an in particular negative output signal (38a), and
 - the output signal (56) of the first phase detector (44) is added to the in particular negative output signal (38a) of the second phase detector (38) by at least a fourth adder (32).
- 10 13. A method as claimed in claim 12, characterized in that, in the event of insufficient accuracy of a system clock period as maximum phase offset between the input signal (50; 50') and the output signal (86d) of the frequency generator (76), there is assigned to the phase locked loop (40) at least a second time-to-digital converter (36)
- which is fed the output signal (86d) of the frequency generator (76) and
 - 15 - the output signal (34) of which is fed to the second phase detector (38).
14. A method as claimed in any of claims 11 to 13, characterized in that
- as a function of at least one switching signal (90), the output signal (92a) of at least a first switching element (92) is switched between the input signal (50; 50') and at least one output signal (86d) of the output signals (86a, 86b, 86c, 86d; 86a', 86b', 86c', 86d', 86e') sent out by the frequency generator (76),
 - the phase detector (44) is fed the output signal (92a) of the first switching element (92),
 - as a function of the switching signal (90), at least a first register element (96),
 - 25 assigned to the input signal (50; 50'), or at least a second register element (98), assigned to the output signal (86d) of the frequency generator (76), is fed the output signal (56) of the phase detector (44) by at least a second switching element (94),
 - as a function of the negated switching signal (90), at least a fourth adder (32) is fed the first output signal (94a1) of the second switching element (94),
 - 30 - as a function of the switching signal (90), the fourth adder (32) is fed the second output signal (94a2) of the second switching element (94), and
 - the output signal (96a) of the first register element (96) is added to the in particular negative output signal (98a) of the second register element (98).

15. A method as claimed in at least one of claims 10 to 14, characterized in that, in the frequency locked loop (10), at least one adaptation unit (14) provides at least one adaptive algorithm and outputs at least one output signal (22), said adaptation unit being fed the increment (24) which is output by the loop filter (30) and being connected between at least one increment module (12), in particular at least one increment generation unit, and the loop filter (30).

16. The use of at least one circuit arrangement (100; 102; 104; 106) as claimed in at least one of claims 1 to 9 and/or of a method as claimed in at least one of claims 10 to 15

10 - in G[lobal]P[ositioning]S[ystem] systems, for example for extracting G[lobal]P[ositioning]S[ystem] signals from at least one G[lobal]P[ositioning]S[ystem] data stream;

- in communication systems, in particular in audio, T[ele]V[ision] and video systems, such as in sound processors, in stereo decoders, in synthesizer tuners and/or in video

15 processors, for example

- to transmit low-frequency signals of additional services in existing services, such as in relation to text in the sync[hronization] signal of at least one television set, and/or

- to control at least one television set from the transmitter, such as in relation to remotely changing image format, volume and/or the like;

20 - in medical technology, for example to activate and/or control at least one pacemaker;

- in measurement technology, for example

- in measurements of speed using ultrasound and/or

- in measurements of distance using ultrasound and/or

25 - to generate signals and/or

- to analyze signals;

- in voice distortion or in voice scrambling, for example

- to modulate voice to at least one changing carrier frequency;

- in telemetry, for example

30 - to demodulate the phase modulation of the input signal (50; 50') and/or

- in a parasitic frequency analysis, that is to say to measure the parasitic phase modulation in the input signal (50; 50').